



**UFE Series of Front End  
Power Supplies**

**Connections Application Note**

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Document Number:

Revision: 0C

Document Status: Draft, Work in Progress

Date: 1/13/2005

Author: Dan Durant

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Preliminary Documentation**

Revision	ECO#	Date	Description of Change
0A		20040805	Document creation
0B		20040924	1) <b>Section 1.1</b> : add Present_L signal to connector with explanation in <b>section 1.1.1</b> 2) Add Appendix B, 18 x UFEPS to 1 x system connector example.
0C		20050113	1) Adjust Figure 1.1 to make more sense (rows vs. columns) 2) Change description of PS-IDX I <sup>2</sup> C addressing bits in <b>section 1.1.1</b>

# 1 UFE Front End Power Supply Connections:

The UFE series of front-end power supplies (referred to from here on simply as “UFEPS”) have many useful connections for a system to interface with. However, not all of these connections are necessary for basic operation of the UFEPS. The AC version UFEPS will use Molex part number 87663-7006, with the recommended use of mating connector 87664-8004. Drawings of these connectors are attached in Appendix A.

## 1.1 UFEPS Small Signal Connections Layout, AC and DC Versions

Figure 1.1 details all of the small signal connections that the UFEPS uses by location grid, for the AC version connector. The DC version, while sharing the same pin functions, may not share the same layout. This grid is laid out as viewed from the connector output side of the UFEPS, as in drawing number 87663-7006, page 1.

Column Row 1-6	#1	#2	#3	#4	#5	#6
D	Sense -	Present-L	PS-ID3	GND	I2C-SDA	GND
C	Sense +	GND	PS-ID2	I2C-SCL	GND	Ishare
B	GND	PS-ID0	GND	PS-ID1	GND	DC-OK-L
A	Short Pin	GND	12V-AUX	GND	I2C-En-H	PS-En

**Figure 1.1: Small Signal Connections Layout, as seen from connector side of UFEPS**

### 1.1.1 Small Signal Connection Definitions

Multiple ground pins are used to minimize noise and cross talk by ensuring a low impedance common signal return path to the UFEPS. The multiple ground pins also provide ESD protection in addition to the internal pin filters and clamps. Having a low impedance path from these ground signals to chassis ground internally in the UFEPS will help force any ESD directed at any of these signal pins away from those potentially damaging paths to chassis and through a harmless path to chassis. Logic “high” on any of these signal pins is considered to be +5V, and logic “low” is considered to be ground or 0V. These “Gnd” Pins should be referenced to chassis ground.

**Short Pin = A1** - This pin is physically shorter than the rest. The purpose of this is for hot swapping the UFEPS. It is the last pin to engage and the first to disengage. For system connection, the mating pin should be grounded. When this ground signal gets into the supply, it enables the micro controller, which in turn enables the rest of the UFEPS.

**12V-AUX = A3** – This pin provides an auxiliary voltage of 11.5V +/- 15% capable of sourcing up to 250mA. It is diode or'ed and may be paralleled with the 12V-AUX pin from other UFEPS's to provide additional power and/or redundancy.

**I2C-En-H = A5** – This pin provides indication that the I<sup>2</sup>C communication has been enabled as well as a means for disabling it. At startup, this pin is pulled high internally. If I<sup>2</sup>C functionality is to be disabled for any reason, such as troubleshooting the I<sup>2</sup>C lines, this pin should be pulled down to ground externally.

**PS-En = A6** – This pin provides an enable function for the supply. At startup this pin is pulled high internal to the UFEPS through a 100K resistor to +5V. To enable the UFEPS, this pin should be pulled low. This can be done with a mechanical switch to ground, an open collector transistor to ground, or a CMOS or TTL compatible logic signal. If this feature is not used, the pin can be permanently grounded in the back plane or mating connector.

**PS-ID0 = B2, PS-ID1 = B4, PS-ID2 = C3, PS-ID3 = D3** – These pins set up the I<sup>2</sup>C addressing that is detailed in the “**I<sup>2</sup>C application note**”. They are pulled high inside the UFEPS to +5V with a 10kOhm resistor and may be grounded externally to change their state to logic low.

**DC-OK-L = B6** – This pin provides an indication that the DC output voltage of the UFEPS, and the 12V-AUX output are both functioning properly. The exact nature of the fault can be determined from the I<sup>2</sup>C system status bits. At startup this pin is pulled high, and as soon as the DC output is enabled and the 12V-AUX voltage is within it's specified range, this pin is pulled low to indicate everything is OK.

**Sense + = C1, Sense - = D1** – These pins provide remote sensing capabilities for the UFEPS. Connecting these at the system load provides automatic compensation for voltage drops from the output of the UFEPS to the system load. This is designed to compensate for at least 0.5V total supply and return drop depending on the output voltage setting. The remote sense lines should be routed separately in a system back plane, or as twisted pair for best results.

**I2C-SCL = C4, I2C-SDA = D5** – These pins provide the I2C data communication lines to the UFEPS as detailed in the “**I<sup>2</sup>C application note**”.

**Ishare = C6** – This pin provides a method for a UFEPS to actively current share with other UFEPS's in a system. This pin should be directly connected to all other Ishare pins in a system if active current sharing will be used. For best results, this signal should be routed directly above a ground plane within a system back plane, or as a twisted pair with an adjacent GND pin. Ground potentials between UFEPS's should be minimized. The only way to enable active current sharing is with the use of I2C, as detailed in the “**I<sup>2</sup>C application note**”.

**Present-L = D2** – This pin provides the capability for determining when a unit is inserted into a system. This pin is pulled low to GND internally in the UFEPS.

## 1.2 UFEPS Power Connections Layout

Figure 2 details all of the power connections that the UFEPS uses by location grid. This grid is laid out as viewed by facing the output connector from the outside of the UFEPS, as in drawing number 87663-7006, page 1.

Power Alpha AC Input Connections (3)			Signal Pins (24)						Power Beta DC Output Connections (4)			
1	2	3	1	2	3	4	5	6	1	2	3	4
AC Line 1	AC Line 2	PEGnd	D	D	D	D	D	D	DC Out -			DC Out +
			C	C	C	C	C	C				
			B	B	B	B	B	B				
			A	A	A	A	A	A				

**Figure 2: Power Connections Layout, as seen from connector side of UFEPS**

### 1.2.1 Power Connection Definitions

**AC Line 1, AC Line 2** – These are the AC input power connections. The input voltage is nominal 230Vac, high range only. Any connection to these lines should be rated for 15A. These connections are also physically shorter than all of the other power connections, for hot-swap and safety considerations. For more details about input power specifications refer to the “UFE series AC-DC Front Ends” main specification.

**PEGnd** – This is the Protective Earth Ground connection required by safety.

**DC Out -, DC Out +** - These are the main DC output connections. Like the signal “Gnd” of the small signal pins, one of these connections, either “DC Out +” or “DC Out -“ should be referenced to chassis ground. The output is capable of either positive or negative polarity.

## 1.3 Connector Pin\Blade Engagement Sequencing

Connector pin\blade engagement sequencing is used to accommodate hot-swap and safety considerations. In the AC UFEPS connector, there are two different lengths of the power blade connectors, as well as two different lengths for the small signal pins.

### 1.3.1 Insertion and Desertion sequencing

Upon insertion into a mating connector, the first connections that are made are the “DC OUT +/-“ and the “PEGnd” blades. Next, the “AC Line 1/2“ blades make a connection. Third to connect are all of the small signal pins except for the “Short Pin”. Finally, the “Short Pin” makes a connection.

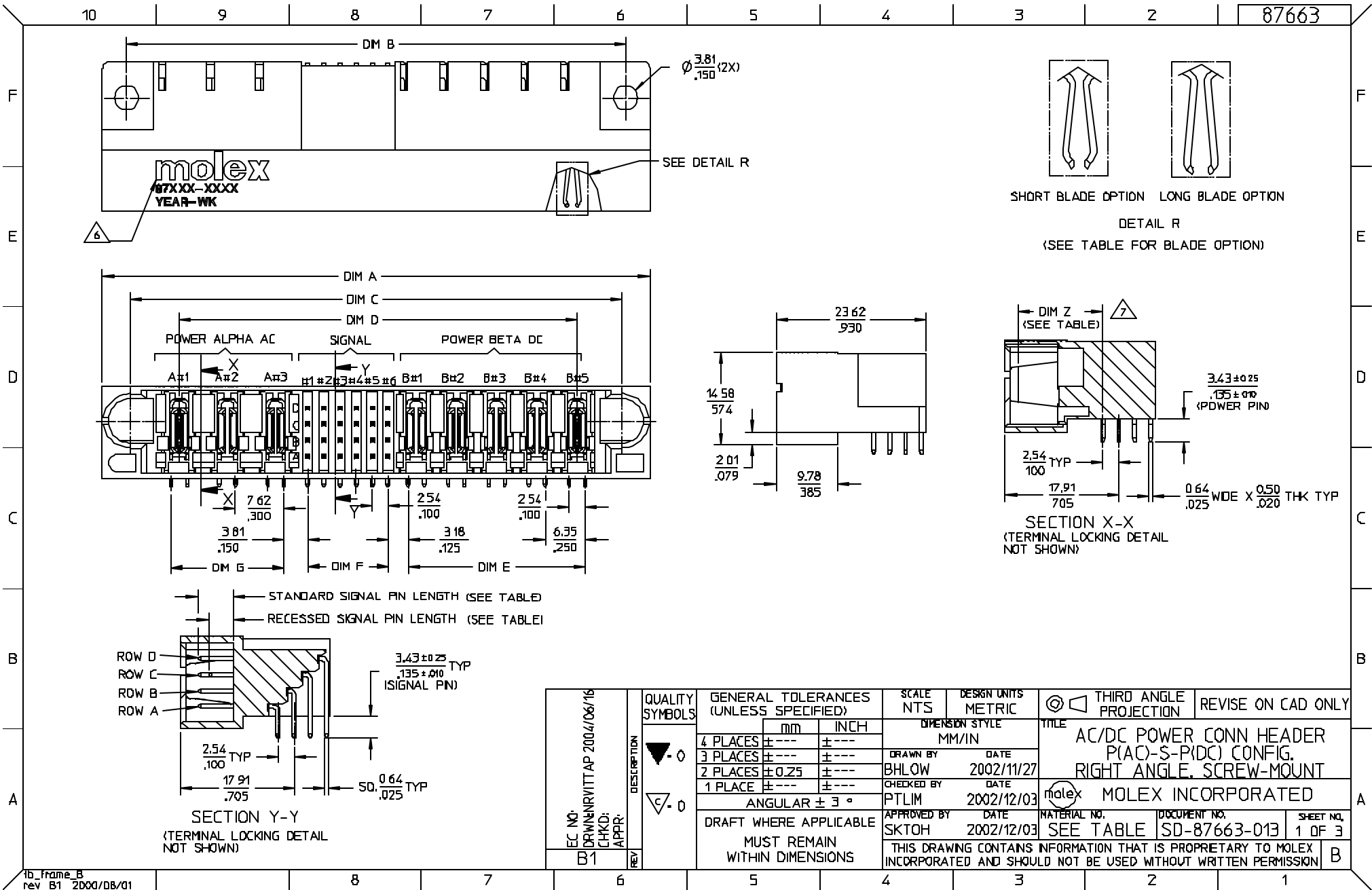


For desertion, this order is simply reversed. The “Short Pin” is the first pin to disconnect, followed by the rest of the signal pins, followed by the “AC Line 1/2 “ blades, and finally the “PEGnd” and “DC OUT +/-“ blades.

## **1.4 Artesyn Designed Chassis Connections**

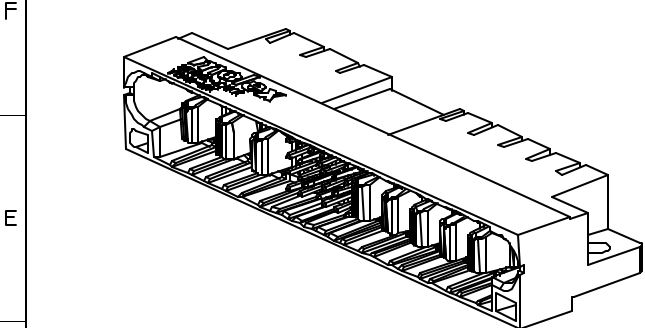
The Artesyn designed chassis takes care of a few of these small signal pins internally, in order to reduce user required involvement. For complete details on the Artesyn designed chassis and the benefits of using it in a system in conjunction with multiple UFEPS’s, refer to the document “**UFEPS Chassis Application Note**” (TBD).

Appendix B also details an example of further reduction from 18 UFEPS’s to one single connection for all of the signal pins.

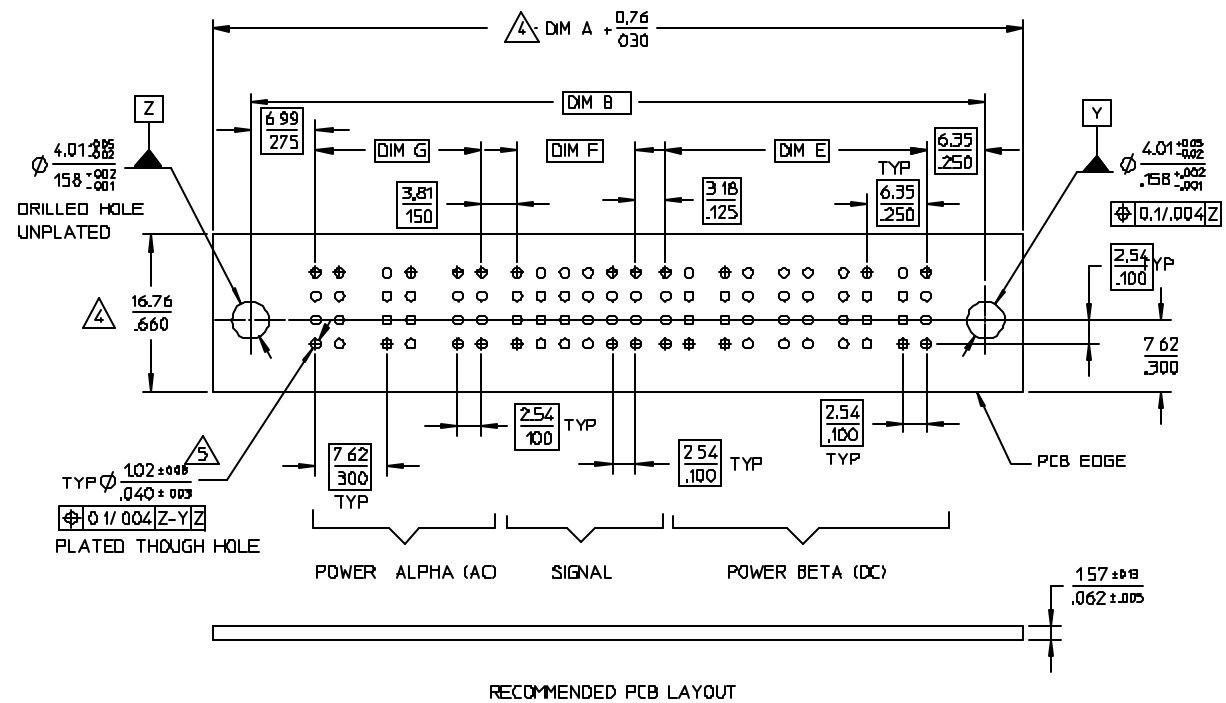


IEC NO: DRWINRVITAP 2004/08/16 CHKD: APPR: B1	QUALITY SYMBOLS - 0 C - 0	GENERAL TOLERANCES (UNLESS SPECIFIED)		SCALE	DESIGN UNITS	THIRD ANGLE PROJECTION REVISE ON CAD ONLY	TITLE AC/DC POWER CONN HEADER P(AC)-S-P(DC) CONFIG. RIGHT ANGLE, SCREW-MOUNT
		MM	INCH	NTS	METRIC		
DESCRIPTION DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS	DIMENSION STYLE MM/IN	4 PLACES	±---	±---	DRAWN BY: BHLW DATE: 2002/11/27	Molex MOLEX INCORPORATED	MATERIAL NO. SEE TABLE DOCUMENT NO. SD-87663-013 SHEET NO. 1 OF 3
		3 PLACES	±---	±---			
		2 PLACES	±0.25	±---	CHECKED BY: PTLIM DATE: 2002/12/03		
		1 PLACE	±---	±---	APPROVED BY: SKTOH DATE: 2002/12/03		
THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION							B

10 9 8 7 6 5 4 3 2



ISOMETRIC VIEW  
3P(AC)-24S-5P(DC) FOR ILLUSTRATION



- NOTES:
- MATERIALS-  
HOUSING - HIGH TEMPERATURE THERMO-PLASTIC,  
GLASS FILLED, UL94V-0, COLOUR: BLACK  
SIGNAL TERMINAL - COPPER ALLOY  
POWER TERMINAL - COPPER ALLOY
  - FINISH -  
SIGNAL & POWER CONTACTS  
0.76 MICROMETER MINIMUM GOLD (Au) AT CONTACT AREA AND  
2.54 MICROMETER MINIMUM TIN (Sn) AT SOLDER TAIL AREA  
OVER 1.27 MICROMETER MINIMUM NICKEL (Ni) UNDERPLATE.
  - PRODUCT SPECIFICATION : PS-87663-006,  
    - COMPONENT STAY AWAY FROM CONNECTOR
    - PCB NOTE FOR DIAMETER 1.02/.040 PLATED HOLE.  
- DRILLED HOLE SIZE IS 1.15 / .0453,  
- PLATE WITH 0.007 / .0003 MINIMUM TIN (Sn) OVER 0.03 / .001  
TO 0.08 / .003 COPPER PLATING TO ACHIEVE 1.02±0.08 / .040±.003 HOLE.
    - MANUFACTURER LOGO, PART NUMBER AND YEAR-WEEK CODE.
    - LONG AND SHORT CONTACT POWER BLADE OPTIONS ARE AVAILABLE FOR  
DIFFERENT CUSTOMERS REQUIREMENT.

IEC NO: DRWINNRVITAPP 2004/08/16 CHKD: LKPKD: APPR: B1 REV:	QUALITY SYMBOLS	GENERAL TOLERANCES (UNLESS SPECIFIED)	SCALE NTS	DESIGN UNITS METRIC	THIRD ANGLE PROJECTION	REVISE ON CAD ONLY
	DESCRIPTION - 0 - C-0	4 PLACES ±--- ±--- 3 PLACES ±--- ±--- 2 PLACES ±0.25 ±--- 1 PLACE ±--- ±--- ANGULAR ± 3 °	MM INCH	DIMENSION STYLE MM/IN	TITLE	
		DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS	DRAWN BY BHLW DATE 2002/11/27	DATE 2002/12/03	AC/DC POWER CONN HEADER P(AC)-S-P(DC) CONFIG. RIGHT ANGLE, SCREW-MOUNT	
			CHECKED BY PTLIM DATE 2002/12/03	DATE 2002/12/03	MOLEX INCORPORATED	
		APPROVED BY SKTOH DATE 2002/12/03	MATERIAL NO. SEE TABLE	DOCUMENT NO. SD-87663-013	SHEET NO. 2 OF 3	
		THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION				B

8 7 6 5 4 3 2 1

### Appendix A: Connector Details



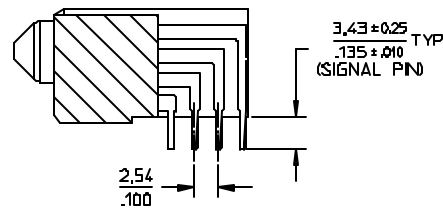
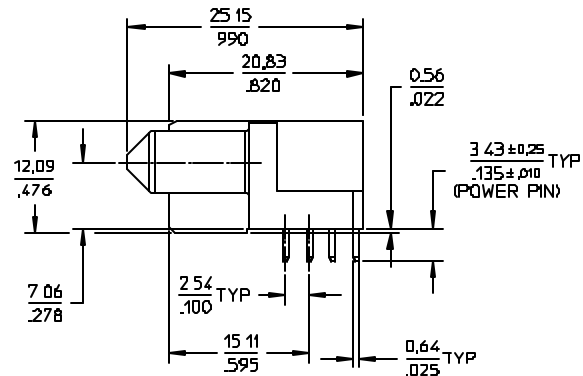
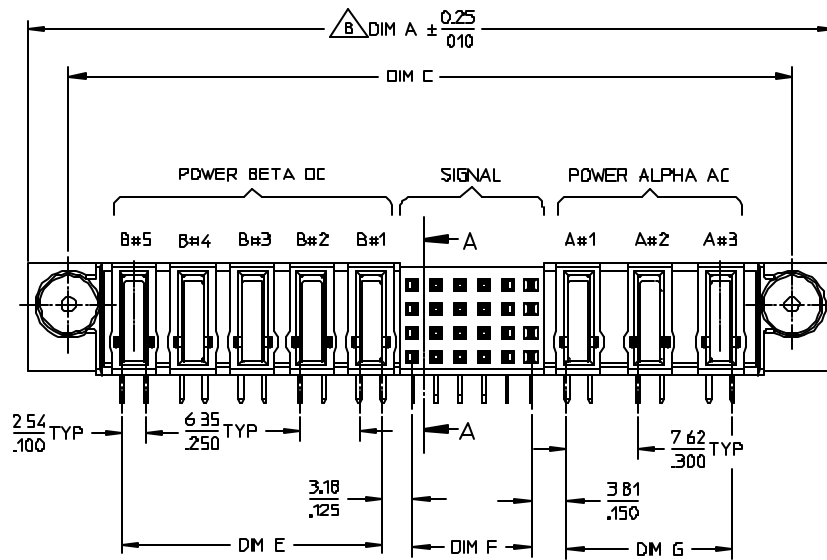
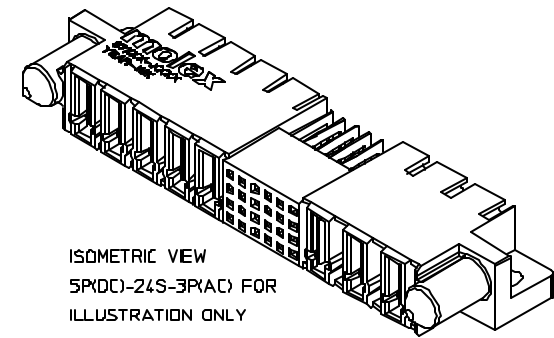
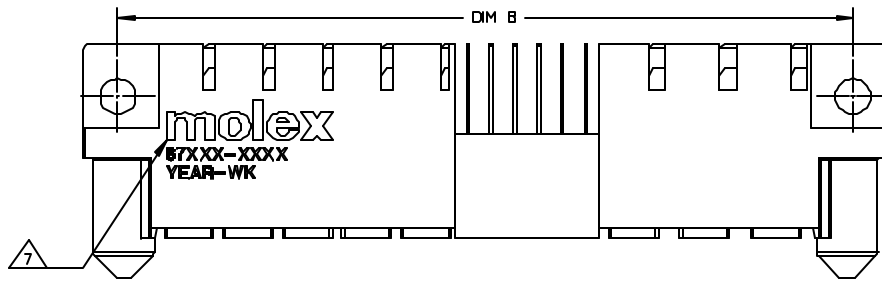
PART NUMBER	P-S-P CONFIGURATION			DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	POWER BLADE OPTIONS		STANDARD SIGNAL PIN LENGTH	RECESSED SIGNAL PIN		PACKAGING
	POWER ALPHA AC	SIGNAL	POWER BETA DC								TYPE	DIM Z ± 0,13/.005		LENGTH	LOCATION	
	3	24	6													
87663-7001	3	24	6	92.71 3.650	85.09 3.350	83.82 3.300	69.22 2.725	34.29 1.350	12.70 .500	17.78 .700	LONG CONTACT	14.12 / .556	6.86/270	5.59/.220	A1	TRAY
87663-7002	3	24	6	92.71 3.650	85.09 3.350	83.82 3.300	69.22 2.725	34.29 1.350	12.70 .500	17.78 .700	LONG CONTACT	14.12 / .556	6.86/270	NIL	NIL	TRAY
87663-7006	3	24	4	80.01 3.150	72.39 2.850	71.12 2.800	56.52 2.225	21.59 0.850	12.70 .500	17.78 .700	LONG CONTACT	14.12 / .556	6.86/270	NIL	NIL	TRAY



IEC NO: DRWINRVITAP 2004/08/16 CHKD: APPR: B1	DESCRIPTION ▼ - 0 ◁ - 0	QUALITY SYMBOLS		GENERAL TOLERANCES (UNLESS SPECIFIED)		SCALE NTS	DESIGN UNITS METRIC	THIRD ANGLE PROJECTION	REVISE ON CAD ONLY	
				mm    INCH			DIMENSION STYLE MM/IN		TITLE AC/DC POWER CONN HEADER P(AC)-S-P(DC) CONFIG. RIGHT ANGLE, SCREW-MOUNT	
		4 PLACES ±--- ±--- 3 PLACES ±--- ±--- 2 PLACES ±0.25 ±--- 1 PLACE ±--- ±---		ANGULAR ± 3 °		DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		DRAWN BY BHLW    DATE 2002/11/27 CHECKED BY PTLIM    DATE 2002/12/03	MATERIAL NO. SEE TABLE    DOCUMENT NO. SD-87663-013    SHEET NO. 3 OF 3	
								APPROVED BY SKTOH    DATE 2002/12/03		THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION

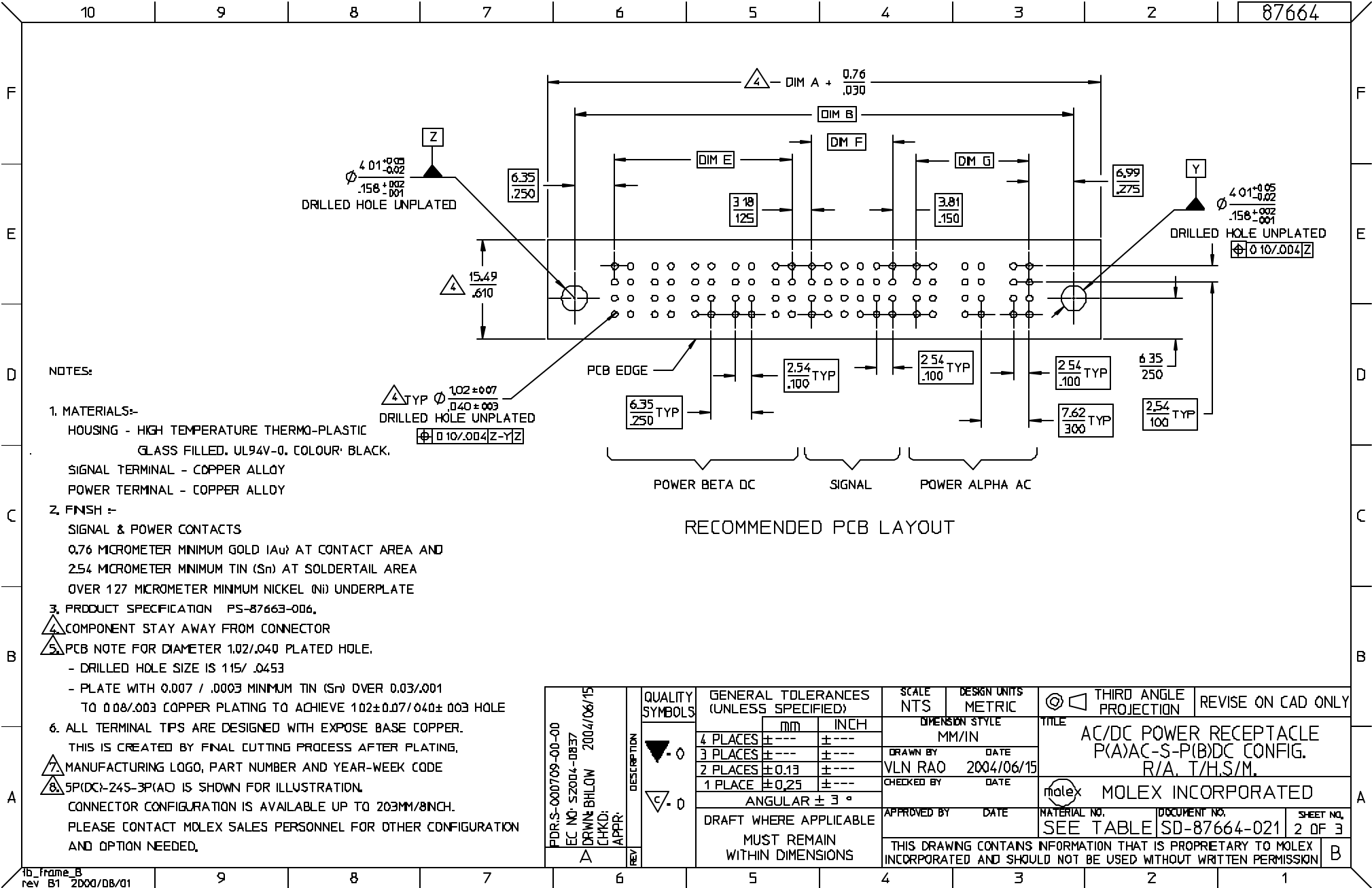
1b\_frame\_B  
rev B1 2001/08/01

Appendix A: Connector Details



SECTION A-A

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		MM	INCH	NTS	METRIC			
		4 PLACES ± ---	± ---	DIMENSION STYLE		TITLE AC/DC POWER RECEPTACLE P(A)AC-S-P(B)DC CONFIG. R/A. T/H/S/M.		
		3 PLACES ± ---	± ---	MM/IN				
2 PLACES ± 0.13	± ---	DRAWN BY	DATE	MOLEX INCORPORATED MATERIAL NO. [ ] DOCUMENT NO. SD-87664-021 SHEET NO. 1 OF 3				
1 PLACE ± 0.25	± ---	VLN RAO	2004/06/15					
ANGULAR ± 3 °		CHECKED BY	DATE	THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION				
DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS		APPROVED BY	DATE					



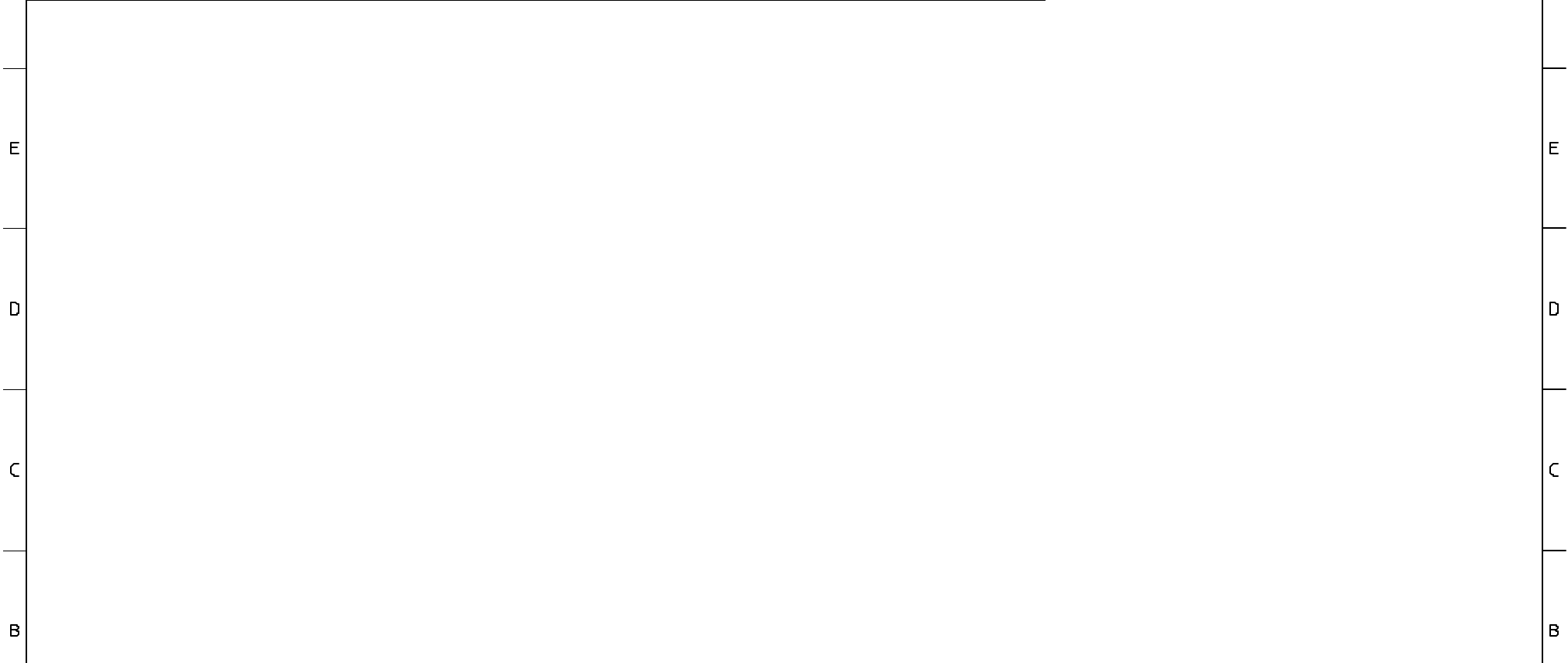
NOTES:

- MATERIALS:-**  
 HOUSING - HIGH TEMPERATURE THERMO-PLASTIC  
 GLASS FILLED, UL94V-0. COLOUR: BLACK.  
 SIGNAL TERMINAL - COPPER ALLOY  
 POWER TERMINAL - COPPER ALLOY
- FINISH :-**  
 SIGNAL & POWER CONTACTS  
 0.76 MICROMETER MINIMUM GOLD (Au) AT CONTACT AREA AND  
 254 MICROMETER MINIMUM TIN (Sn) AT SOLDER TAIL AREA  
 OVER 127 MICROMETER MINIMUM NICKEL (Ni) UNDERPLATE
- PRODUCT SPECIFICATION PS-87663-006.**  
 COMPONENT STAY AWAY FROM CONNECTOR  
 PCB NOTE FOR DIAMETER 1.02/.040 PLATED HOLE.  
 - DRILLED HOLE SIZE IS 115/ .0453  
 - PLATE WITH 0.007 / .0003 MINIMUM TIN (Sn) OVER 0.03/.001  
 TO 0.08/.003 COPPER PLATING TO ACHIEVE 102±0.07/.040±.003 HOLE
- ALL TERMINAL TIPS ARE DESIGNED WITH EXPOSE BASE COPPER.**  
 THIS IS CREATED BY FINAL CUTTING PROCESS AFTER PLATING.
- MANUFACTURING LOGO, PART NUMBER AND YEAR-WEEK CODE**
- SP(DC)-245-3P(AC) IS SHOWN FOR ILLUSTRATION.**  
 CONNECTOR CONFIGURATION IS AVAILABLE UP TO 203MM/8INCH.  
 PLEASE CONTACT MOLEX SALES PERSONNEL FOR OTHER CONFIGURATION  
 AND OPTION NEEDED.

RECOMMENDED PCB LAYOUT

FDR: S-000709-00-00 IEC NO: S2004-0837 DRAWN BY: BILLOW 2004/06/15 CHKD: [blank] APPR: [blank]	QUALITY SYMBOLS - O C- O	GENERAL TOLERANCES (UNLESS SPECIFIED)		SCALE	DESIGN UNITS	THIRD ANGLE PROJECTION	REVISE ON CAD ONLY		
				NTS	METRIC				
				DIMENSION STYLE		TITLE			
				MM/IN		AC/DC POWER RECEPTACLE P(A)AC-S-P(B)DC CONFIG. R/A. T/H/S/M.			
		4 PLACES ±---		DRAWN BY		DATE			
		3 PLACES ±---		VLN RAO		2004/06/15			
		2 PLACES ±0.13		CHECKED BY		DATE			
		1 PLACE ±0.25		MOLEX MOLEX INCORPORATED					
		ANGULAR ± 3 °		APPROVED BY		DATE			
		DRAFT WHERE APPLICABLE		MATERIAL NO.		DOCUMENT NO.			
		MUST REMAIN WITHIN DIMENSIONS		SEE TABLE		SD-87664-021			
				THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION		SHEET NO. 2 OF 3			

	10	9	8	7	6	5	4	3	2	87664			
	P-S-P CONFIGURATION												
	PART NUMBER	POWER BETA DC	SIGNAL	POWER ALPHA AC	DM A	DM B	DIM C	DIM D	DIM E	DIM F	DIM G	RECESSED POWER PIN LOCATION	PACKAGING
F	87664-8004	3	24	4	$\frac{80.01}{3.150}$	$\frac{72.39}{2.850}$	$\frac{71.12}{2.800}$	$\frac{56.52}{2.225}$	$\frac{21.59}{0.850}$	$\frac{12.70}{.500}$	$\frac{17.78}{.700}$	A B	2, 3 ----- TRAY

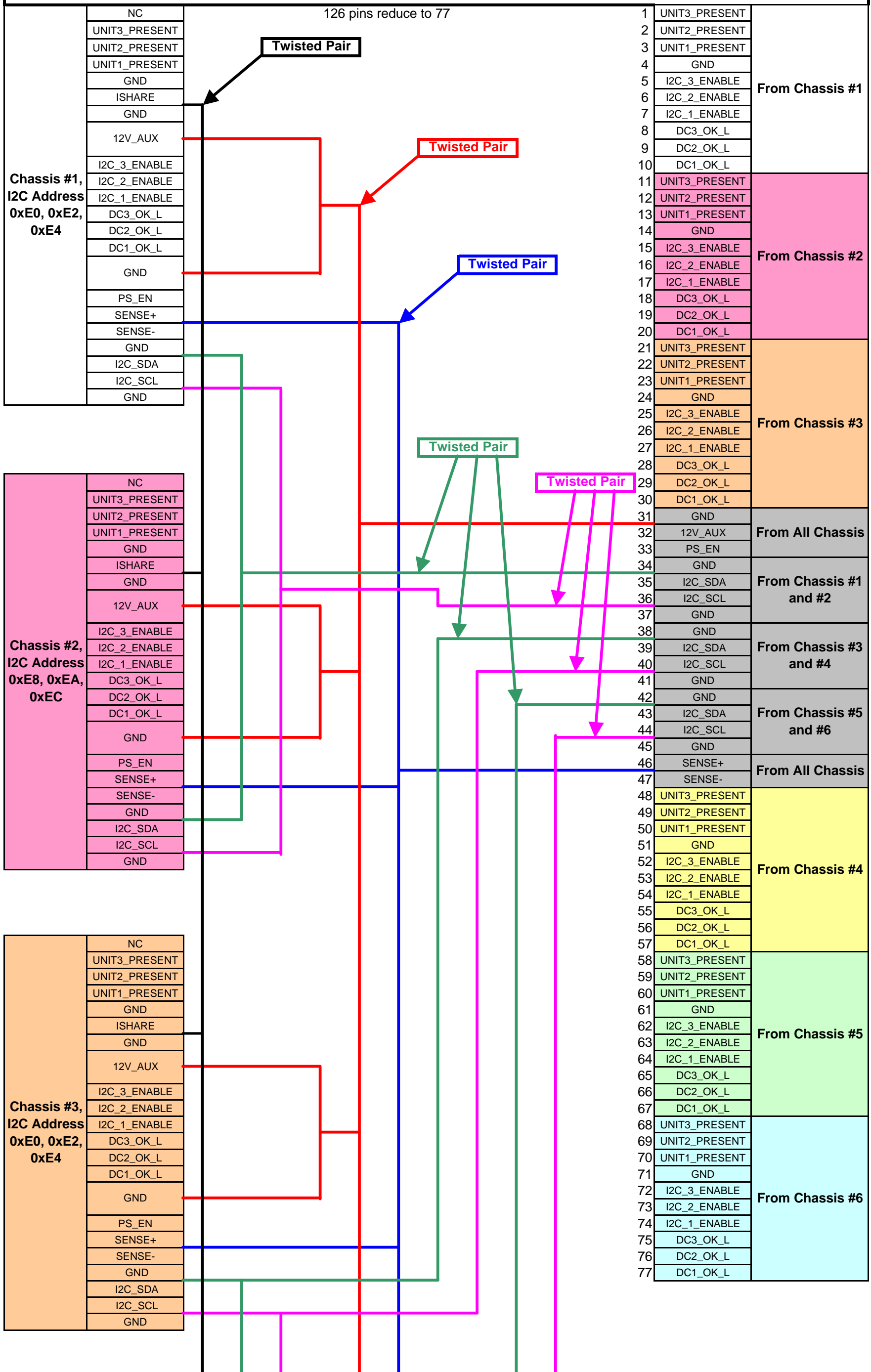


PDR: 5-060709-00-00 EC NO: S2004-0837 DRAWN BY: DRVINBHLOW 2004/06/15 CHKD: [blank] APPR: [blank]	QUALITY SYMBOLS	GENERAL TOLERANCES (UNLESS SPECIFIED)	SCALE NTS	DESIGN UNITS METRIC	THIRD ANGLE PROJECTION	REVISE ON CAD ONLY	
		MM	INCH	DIMENSION STYLE MM/IN		TITLE AC/DC POWER RECEPTACLE P(A)AC-S-P(B)DC CONFIG. R/A. T/H/S/M.	
		4 PLACES ±---	±---	DRAWN BY DATE			
		3 PLACES ±---	±---	VLN RAO 2004/06/15			
		2 PLACES ±0.13	±---	CHECKED BY DATE			
1 PLACE ±0.25	±---	ANGULAR ± 3 °		MOLEX INCORPORATED			
	DRAFT WHERE APPLICABLE MUST REMAIN WITHIN DIMENSIONS	APPROVED BY DATE	MATERIAL NO.	DOCUMENT NO.	SHEET NO.		
			SEE TABLE	SD-87664-021	3 OF 3		
		THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX INCORPORATED AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION					

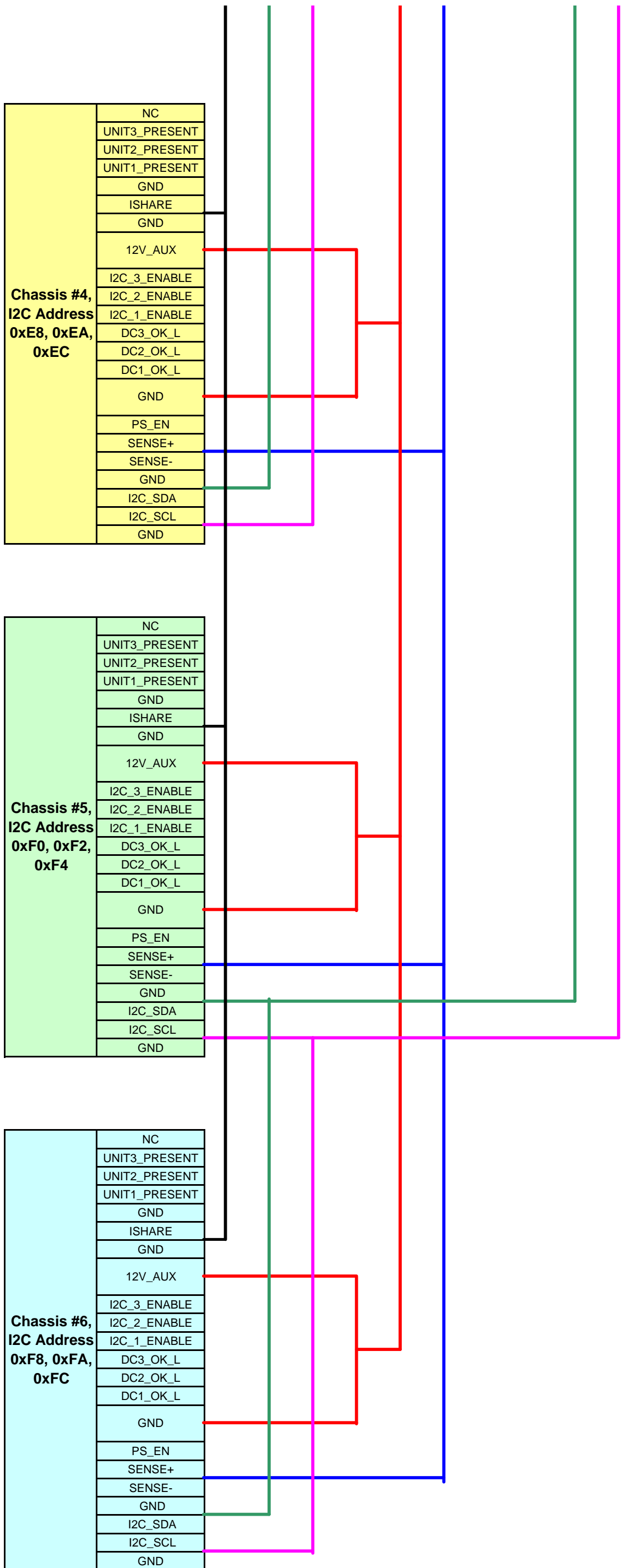
10	9	8	7	6	5	4	3	2	1
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## Appendix A: Connector Details

# Recommended connection scheme for a 6 chassis (18 UFEPs) system



Appendix B: Example Connections Reduction, 18 x UFEPs to Single Connector



Appendix B: Example Connections Reduction, 18 x UFEPS to Single Conneciton